

326	39	Subclass
ISSUE CLASSIFICATION		

PATENT NUMBER

U.S. REISSUE Patent Application

<p>O.I.P.E.</p> <p>SCANNED <i>10-2</i> G.A. <i>Am</i></p>	<p>O.G. PUBLICATION DATE</p> <p>1-29-02</p>	<p>REISSUE PATENT DATE</p>
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APPLICATION NO. 09/963735	CONT/PRIOR D F	CLASS 326	SUBCLASS 39	ART UNIT 2819	EXAMINER D Le
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APPLICANTS

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Semiconductor integrated circuit with mixed gate array and standard cell

PTO-2040
12/89

☒ SURRENDER OF ORIGINAL PATENT (Ext. Initials)

ORIGINAL PATENT NUMBER 6054,872

ISSUING CLASSIFICATION

ORIGINAL						CROSS REFERENCE(S)								
CLASS		SUBCLASS		CLASS		SUBCLASS (ONE SUBCLASS PER BLOCK)								
326		39		326		101								
INTERNATIONAL CLASSIFICATION														
H03K 19/177														
						<input type="checkbox"/> Continued on Issue Slip inside File Jacket								

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg. <u>17</u>	Figs. Drwg. <u>18</u>	Print Fig. <u>3A</u>	Total Claims <u>65</u>	Print Claim for O.G. <u>30</u>
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed. <input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____ <input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED	
	DON LE PRIMARY EXAMINER <u>X</u> (Primary Examiner) <u>5/7/83</u> (Date)			ISSUE FEE	
				Amount Due	Date Paid
FINAL SPRE REVIEW _____ (INITIALS)	_____ (Legal Instruments Examiner) (Date)			ISSUE BATCH NUMBER	

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